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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/984,560	12/03/1997	JEFFEREY S. MAILLOUX	95-0653.01	2301

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EXAMINER	
KIM, HONG CHONG	
ART UNIT	PAPER NUMBER
2187	25

DATE MAILED: 07/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/984,560	Maillouk et al
Examiner	Group Art Unit
H. Kim	2187

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 10/30/01.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 11-21 + 59-71 is/are pending in the application.

Of the above claim(s)_____ is/are withdrawn from consideration.

☐ Claim(s)_____ is/are allowed.

☒ Claim(s) 11-21 + 59-71 is/are rejected.

☐ Claim(s)_____ is/are objected to.

☐ Claim(s)_____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on_____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on_____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)_____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:_____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 23

☐ Interview Summary, PTO-413

☐ Notice of References Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other_____

Office Action Summary

Detailed Action

1. Claims 11-21 and 59-71 are presented for examination. This office action is in response to the amendment filed on 5/10/30/01.

2. Receipt is acknowledged of information disclosure statement filed on 10/16/01, which the statement has been placed of record in the file. Information disclosed and listed on PTO 1449 was considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 11-21 and 59-71 are rejected under 35 USC 102(b) as being anticipated by *Manning*, U.S. Patent 5,610,864.

As to claim 11, *Manning* discloses the invention as claimed. *Manning* discloses a storage device comprising: control logic (Fig. 1 Ref. 38 and col. 6 lines 26-32) for between a patternless

addressing scheme (col. 5 lines 43-50) and a patterned addressing scheme (col. 6 lines 14-26 and col. 7 lines 43-54) and switching circuit for switching between a first pathway and a second pathway (Fig. 1 Ref. 38 and col. 5 lines 43-50, col. 6 lines 14-32 & col. 7 lines 43-54).

As to claim 12, Manning further discloses the storage device is asynchronous (Fig. 1 and EDO constitutes asynchrous memory, col. 4 line 17).

As to claim 13, Manning further discloses temporary buffer (Fig. 1 Refs. 18 and 34).

As to claim 14, Manning further discloses the external address is temporarily stored in the temporary storage device prior to being sent to a decoder (Fig. 1 Refs. 12 and 30).

As to claim 15, Manning further discloses counter (Fig. 1 Ref 26).

As to claim 16, Manning further discloses the internal address is provided to temp storage device through the switching circuitry (Fig. 1 Refs. 38, 40, 26, 34).

As to claim 17, Manning further discloses a pipeline mode (col. 5 lines 43-50).

As to claim 18, Manning further discloses a burst mode (col. 7 lines 28+).

As to claim 19, Manning further discloses muxes (Fig. 5 Refs. 58, 61 and 66).

As to claim 20, Manning further discloses patternless addressing scheme is for random CAS (col. 5 lines 43-50) and the patterned addressing scheme is for sequence CAS (col. 6 lines 14-26 and col. 7 lines 43-54).

As to claim 21, Manning further the sequence CAS is selected from a group consisting of interleaved (col. 4 lines 56-57) and linear column address access (col. 4 line 56).

As to claims 59 and 60, *Manning* discloses the invention as claimed. *Manning* discloses a memory device, comprising:

a memory array (Fig. 1 Ref. 12);

control logic operatively connected to the memory array, the control circuit for selecting between an unpatterned pipeline (col. 5 lines 43-50) and a patterned burst data pattern (col. 6 lines 14-26 and col. 7 lines 43-54) for accessing the memory array; and

switching circuit for switching between a first, burst data pathway and a second, pipeline data pathway depending on which of the burst or pipeline modes of operation is selected (Fig. 1 Ref. 38 and col. 5 lines 43-50, col. 6 lines 14-32 & col. 7 lines 43-54).

As to claim 61, *Manning* discloses the invention as claimed above. *Manning* further discloses a column address decoder for receiving an external column address (Fig. 1 Ref. 30).

As to claim 62, *Manning* discloses the invention as claimed above. *Manning* further discloses a counter (Fig. 1 Ref. 26) and switching circuit for switching between a first pathway and a second pathway depending on which of the patternless addressing scheme or patterned addressing scheme is selected (Fig. 1 Ref. 38 and col. 5 lines 43-50, col. 6 lines 14-32 & col. 7 lines 43-54), wherein the first pathway and the second pathway are coupled to a temporary storage device for providing at least one external address (Fig. 1 Ref. 16) to the switching circuitry, and wherein the counter is coupled tp the temporary storage device to receive a selected portion of the external address for generating an internal address (col. 8 line 45).

As to claim 63, *Manning* discloses the invention as claimed above. *Manning* further discloses the internal address is provided to the temporary storage device through the switching circuitry (Fig. 1 Refs. 18 and 26).

As to claim 64, *Manning* discloses the invention as claimed above. *Manning* further discloses the patternless addressing scheme provides a pipeline extended data out pattern (col. 5 lines 43-50).

As to claim 65, *Manning* discloses the invention as claimed. *Manning* discloses a storage device, comprising:

control logic for selecting between a patternless addressing scheme (col. 5 lines 43-50) and a patterned addressing scheme (col. 6 lines 14-26 and col. 7 lines 43-54); and

switching circuit for switching between a first pathway and a second pathway depending on which of the patternless addressing scheme or patterned addressing scheme is selected (Fig. 1 Ref. 38 and col. 5 lines 43-50, col. 6 lines 14-32 & col. 7 lines 43-54), wherein the pattenless addressing scheme provides a pipelined extended data out pattern (col. 5 lines 43-50).

As to claim 66, *Manning* discloses the invention as claimed above. *Manning* further discloses the patterned addressing scheme provide a burst extended data out pattern (col. 6 lines 14-26 and col. 7 lines 43-54)

As to claim 67, Manning further discloses at least one multiplexed device (Fig. 5 Refs. 58, 61 and 66).

As to claim 68, *Manning* discloses the invention as claimed. *Manning* discloses a storage device, comprising:

control logic for selecting between a patternless addressing scheme (col. 5 lines 43-50) and a patterned addressing scheme (col. 6 lines 14-26 and col. 7 lines 43-54); and

switching circuit for switching between a first pathway and a second pathway depending on which of the patternless addressing scheme or patterned addressing scheme is selected (Fig. 1 Ref. 38 and col. 5 lines 43-50, col. 6 lines 14-32 & col. 7 lines 43-54), wherein the patterned addressing scheme provide a burst extended data out pattern (col. 6 lines 14-26 and col. 7 lines 43-54).

As to claim 69, Manning further discloses at least one multiplexed device (Fig. 5 Refs. 58, 61 and 66).

As to claim 70, *Manning* discloses the invention as claimed. *Manning* discloses a memory device, comprising:

a memory array (Fig. 1 Ref. 12) operable in a burst or a pipelined mode of operation (col. 6 lines 14-26, col. 7 lines 43-54, and col. 5 lines 43-50);

control logic for selecting between a the pipeline mode of operation (col. 5 lines 43-50) and the burst mode of operation (col. 6 lines 14-26 and col. 7 lines 43-54); and

switching circuit for switching between a first, burst data pathway and a second, pipeline data pathway depending on which of the burst or pipeline modes of operation is selected (Fig. 1 Ref. 38 and col. 5 lines 43-50, col. 6 lines 14-32 & col. 7 lines 43-54), wherein the first pathway and the second pathway are coupled to a temporary storage device for providing at least one external address (Fig. 1 Ref. 16) to the switching circuitry.

As to claim 71, Manning further discloses a counter coupled to the temporarily storage device to receive a selected portion of the external address for generating an internal address (Fig. 1 Refs. 26 and 30).

Response to Arguments

5. Applicant's arguments filed on 10/30/01 have been fully considered but they are not persuasive.

Applicant's argument on page 2 that the reference does not disclose switching circuit for switching between a first pathway and a second pathway is not considered persuasive.

Manning discloses switching circuit for switching between a first pathway and a second pathway (Fig. 1 Ref. 38 and col. 5 lines 43-50, col. 6 lines 14-32 & col. 7 lines 43-54).

Applicant's argument on page 3 that the reference does not disclose selecting between a burst mode and a pipeline modes of operations is not considered persuasive.

"The current invention include a pipelined architecture" (col. 5 lines 43-49 in Manning) and "switching between standard fast page mode (non-EDO) and burst mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) read on this limitation, in other words, in order to work in the pipeline architecture one has to select pipeline mode. Also given the teachings of above reference one of the ordinary skill in the art at the time the invention was made would have been lead to an obvious fashion to provide a pipelined page mode circuitry since Manning discloses that the current invention include a pipelined architecture (col. 5 lines 43-49) which

would increase accessing speed. Also Ryan US Patent 5,966,724 discloses additional column addresses are latched and access are performed in a pipelined page mode (col. 4 lines 22-24). Therefore, broadly written claims are disclose by the references cited.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., enabling switching between pipeline or burst operations with in the same memory, "on-the-fly") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Therefore broadly written claims are disclosed by the references cited.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

8. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

9. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

10. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100:
After-final (703) 746-7238
Official (703) 746-7239 (for formal communications intended for entry)

Non-Official/Draft (703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Primary Patent Examiner
July 23, 2002

HONG CHONG KIM
PRIMARY EXAMINER